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200 Ω Chopper Driver Progress

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PIP-II Technical Meeting

29 March 2016

Acknowledgements:
Jeff Simmons

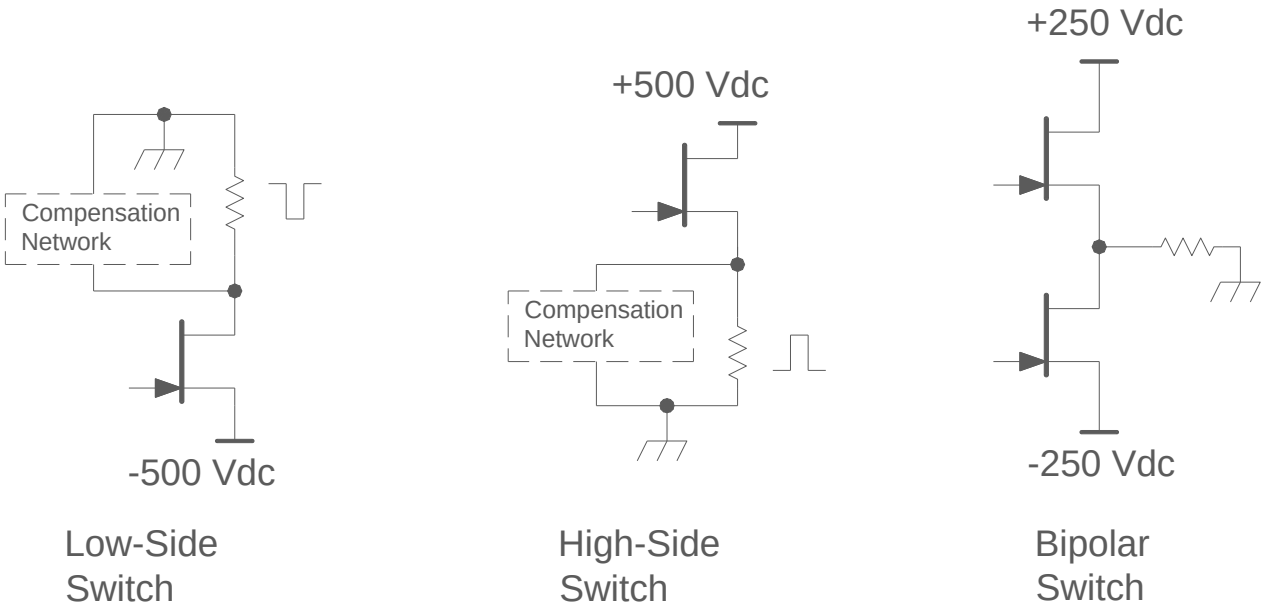
Topics

- Review of driver requirements
- Current development status
- Some performance results
- Thermal issues at high switching rates

200 Ω Chopper Driver design

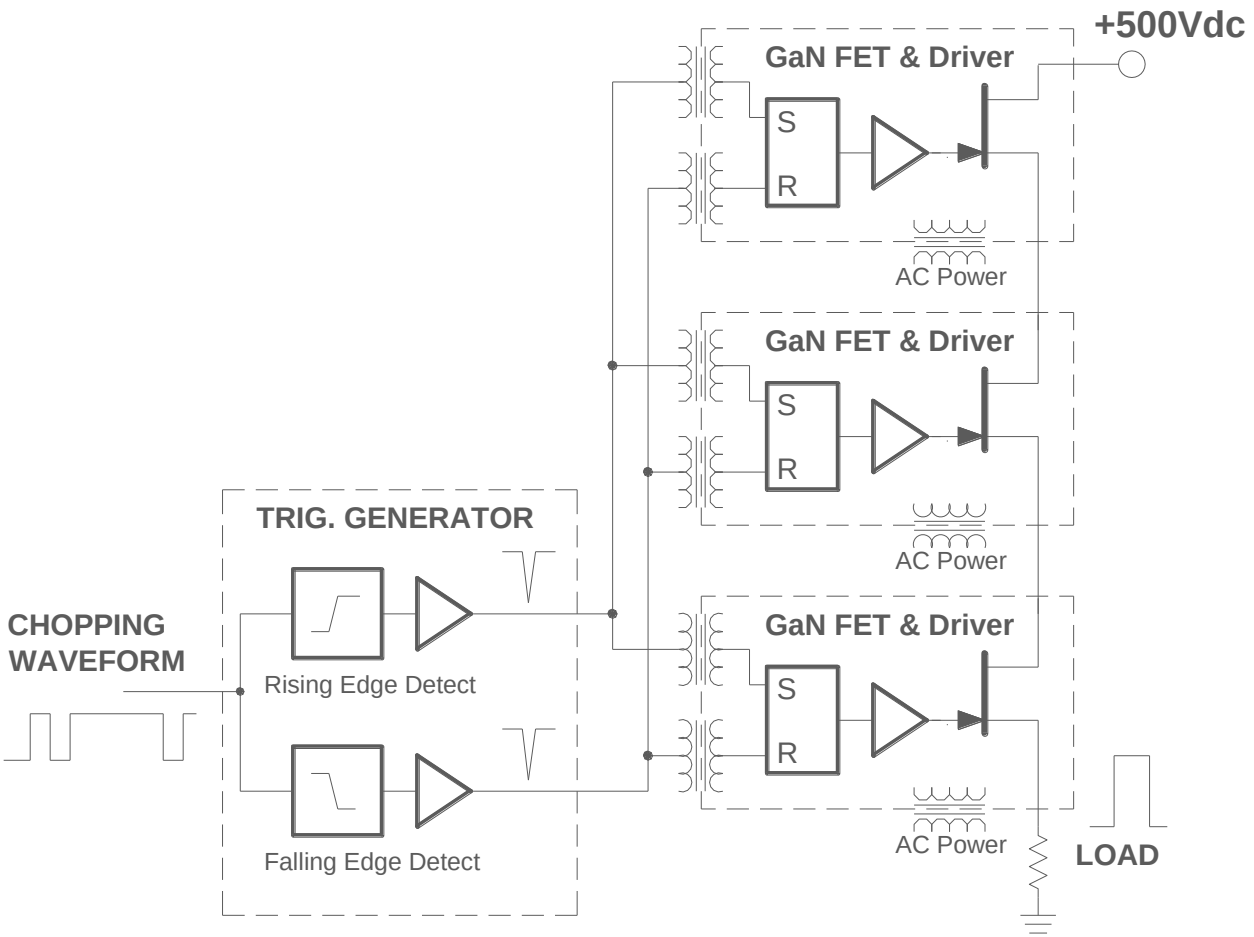
- PIP-II CW machine requirements expressed in terms of a driver built as a switch
  - Operating voltage: 500 V min.
  - Pulse width range: ~2.2 ns flat top width to >1 μs
  - Max acceptable rise/fall time: 4.5 ns, 5 - 95%
  - Max rep rate: 81 MHz for short bursts (kick every other bunch)
  - Average switching rate: ~35 MHz
- Switch design approach (benefiting from LDRD program)
  - 650 V GaN FETs used (GaN Systems)
  - Each FET and its driver circuit – a "stage"
    - Triggered individually
    - All stages are matched for turn-on and turn-off delay, and turn-on rise time (+/- ~0.2 ns)
  - Isolated AC/DC power supply system developed
    - Each stage requires well regulated voltages
    - Power available is ~3 Watts to each stage
  - Two FET driver circuits developed:
    - "Rev_B" achieved ~3 ns turn-on time
    - "Rev_C" achieved ~1.5 ns turn-on time
  - Isolated trigger generator system used transformers
    - No semiconductor solution can handle required transient immunity
    - Low enough fiber optic solutions are too big and bulky
  - 3-FET stage switches operate at 630 V
  - Anticipate 3 or 4 stages per switch

Isolated switch provides topology options



- The compensation network is required to decrease the turn-off time
  - Turn-off times reduced by 50%
- Low- and high-side switch may, or may not, be practical at high duty factors

Chopper Driver system (as a high-side switch)



GaN FET used

GaN Systems

GS66502B
Bottom-side cooled 650 V E-mode GaN transistor
Preliminary Datasheet

Features

- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 200 mΩ
- $I_{DS(max)}$ = 7.5 A
- Ultra-low FOM Island Technology® die
- Low inductance GaNPX™ package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 5.0 x 6.6 mm^2 PCB footprint
- RoHS 6 compliant

Key specs:

BV_{DS} = 650 V

$I_{DS(DC)}$ = 7.5 A

$I_{DS(pulse)}$ = 15 A

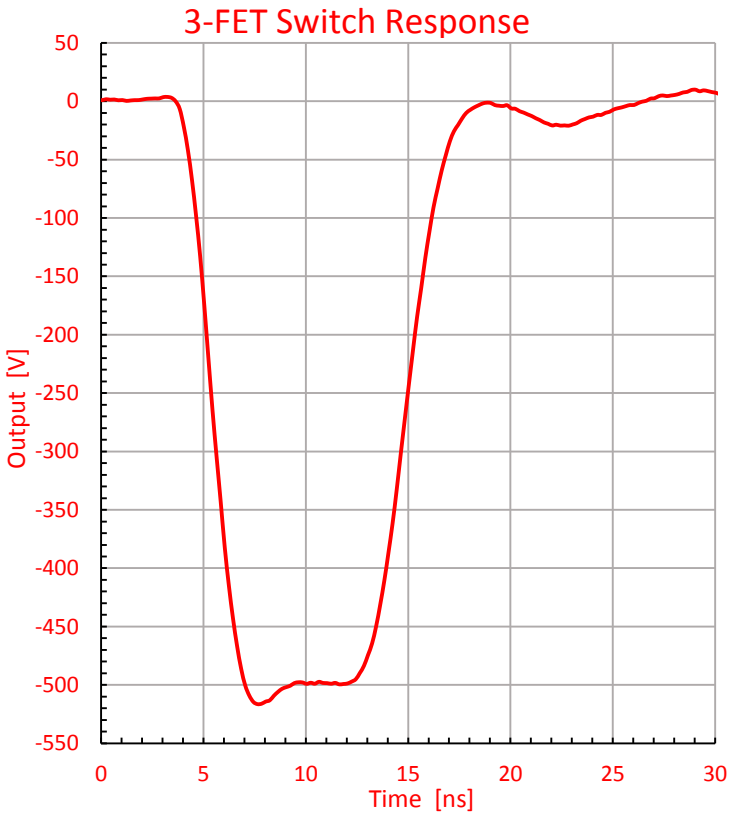
C_{iss} = 65 pF

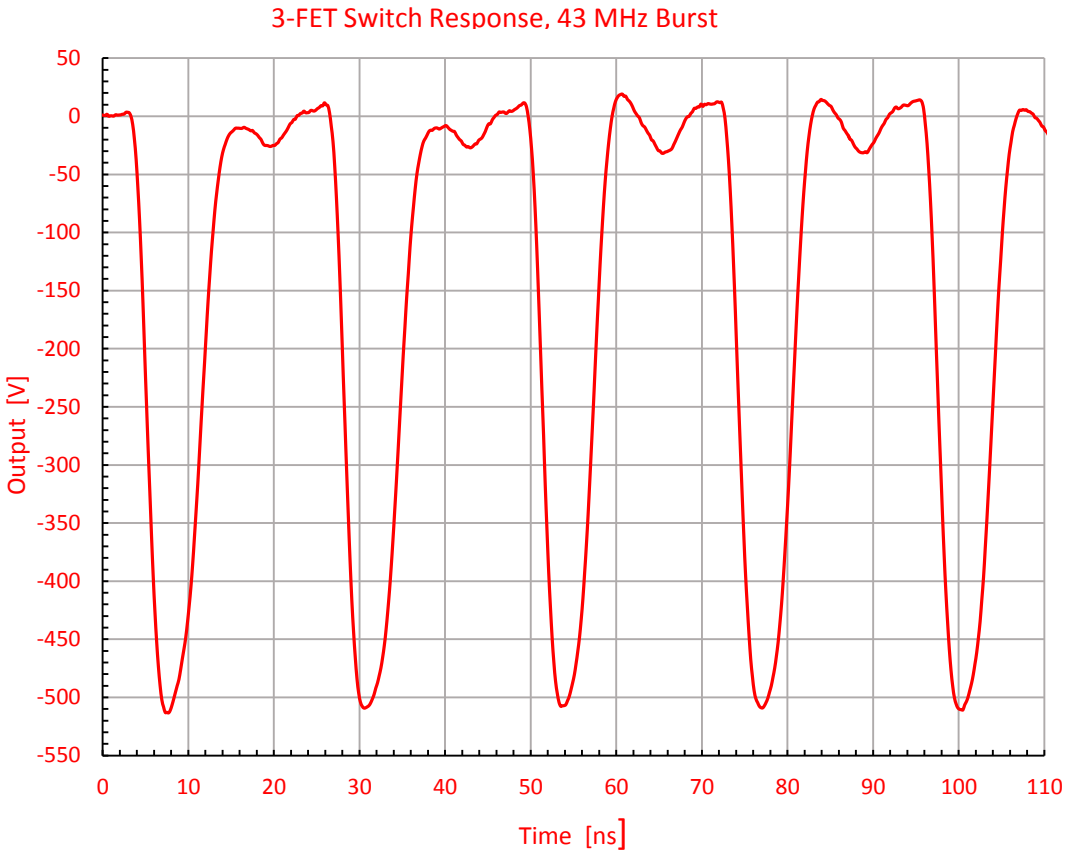
C_{oss} = 17 pF

C_{rss} = 0.5 pF

$R_{DS(on)}$ = 200 mΩ

3-Stage switch, low-side switch





Max. operation: 630 V
Load: 185 Ω
turn-on time: 3.0 ns
turn-off time : 4.0 ns
Flat top pulse width: 2.2 ns to infinity

Switch built using “Rev_B” driver version

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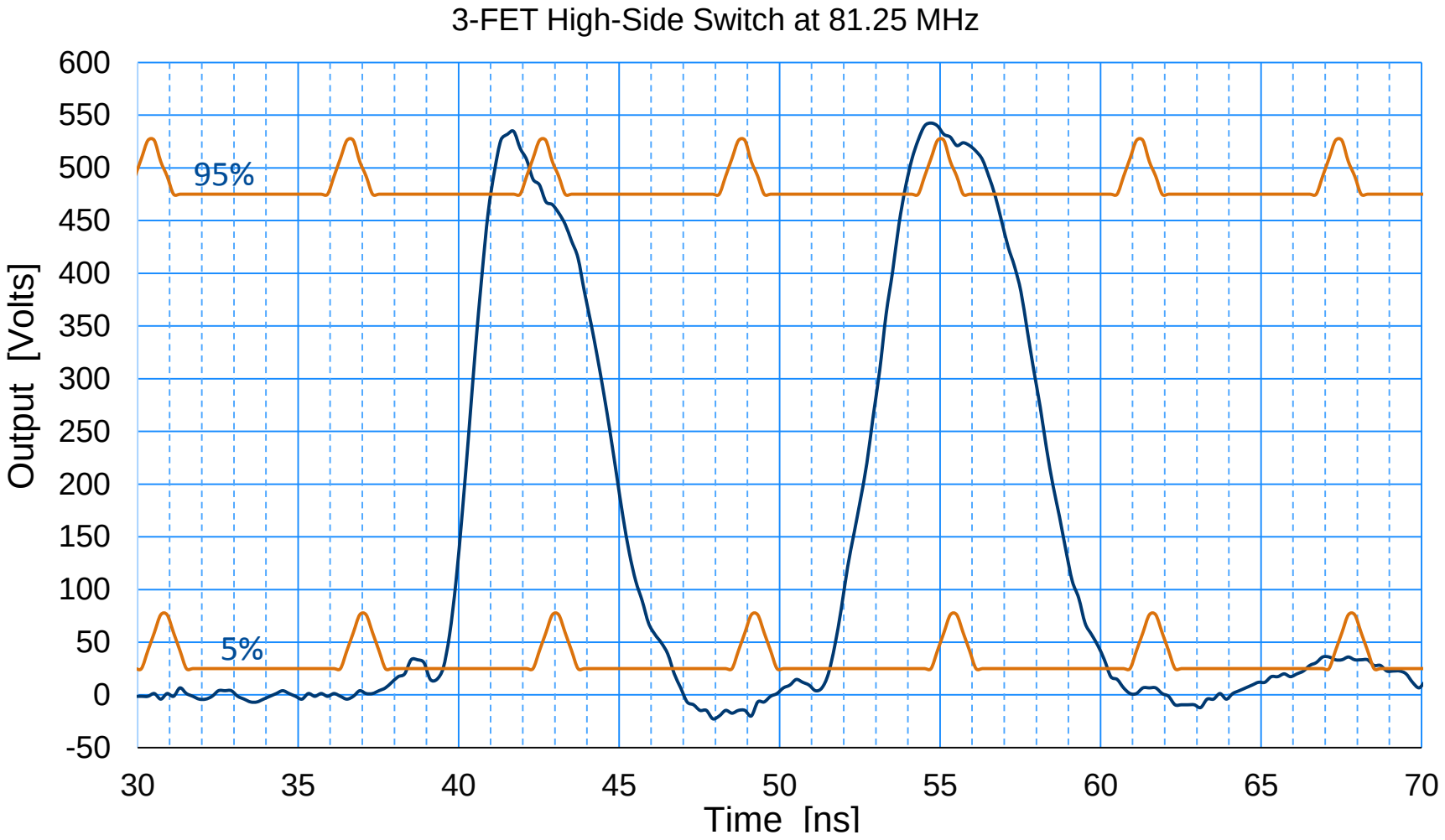
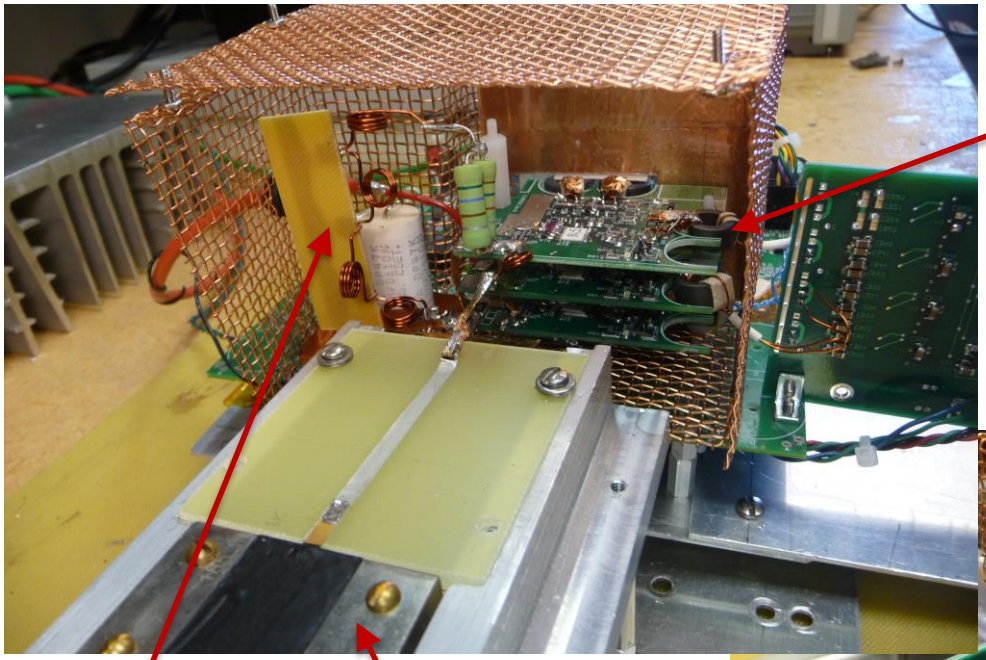
3-Stage switch, high-side switch



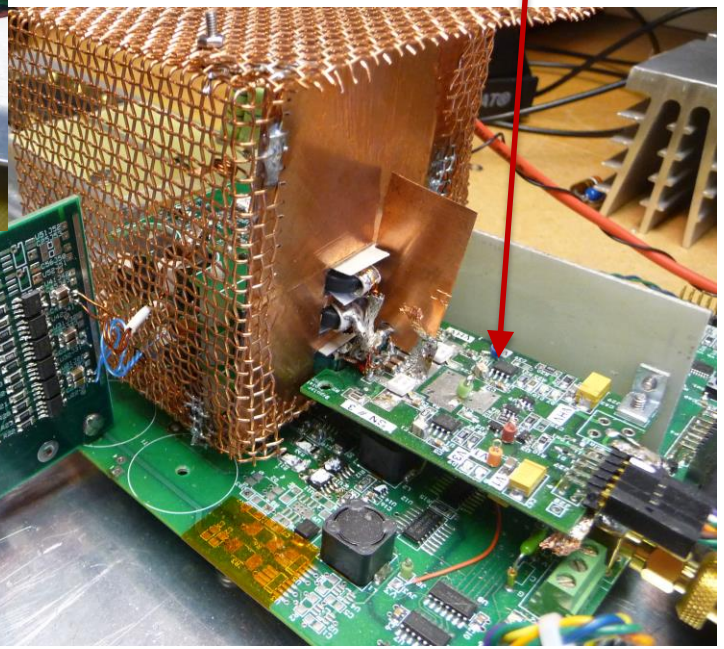
- Beam bunches are superimposed on tolerance limit lines
- Switch built using “Rev_C” driver version

Switch built with “Rev_B” drivers



3-Stage switch

Trig. generator

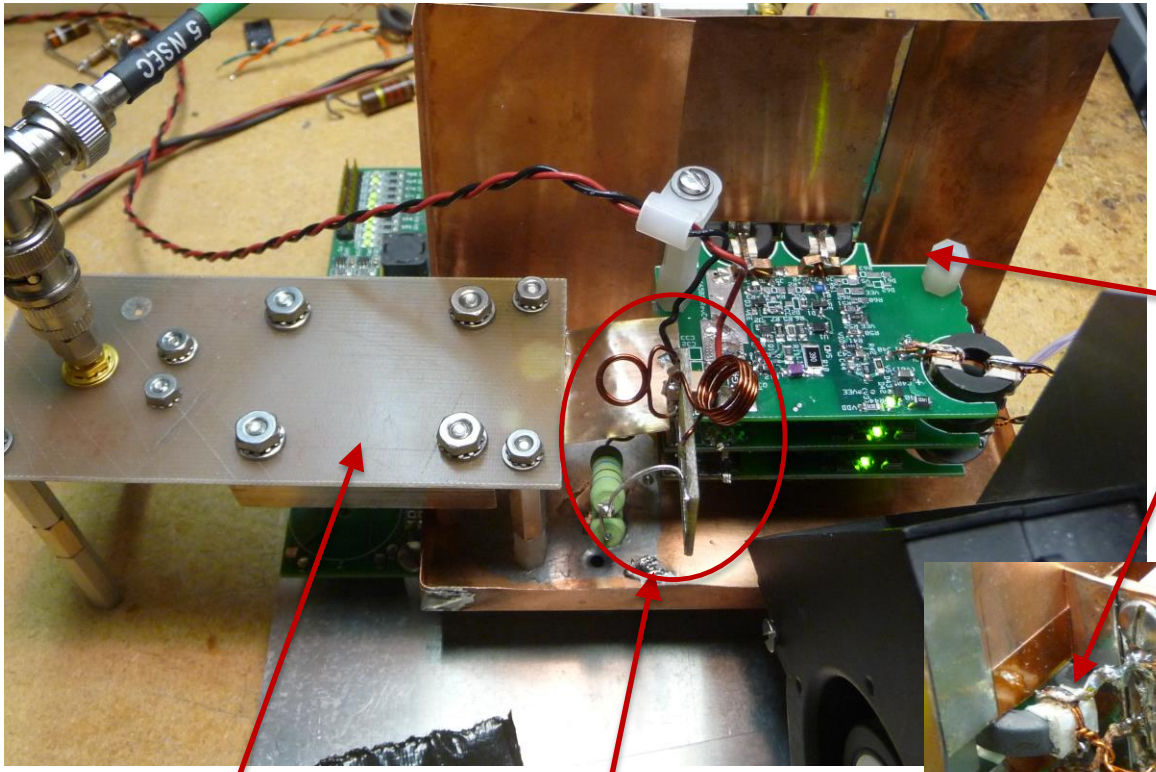


Comp. network

185 Ω load

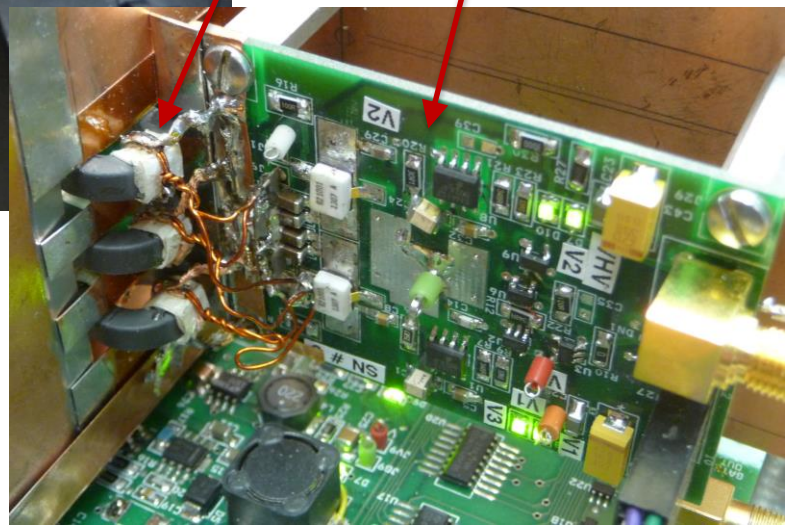
AC power supply bd.

Switch built with “Rev_C” drivers



Trig. transformers
(2 per driver)

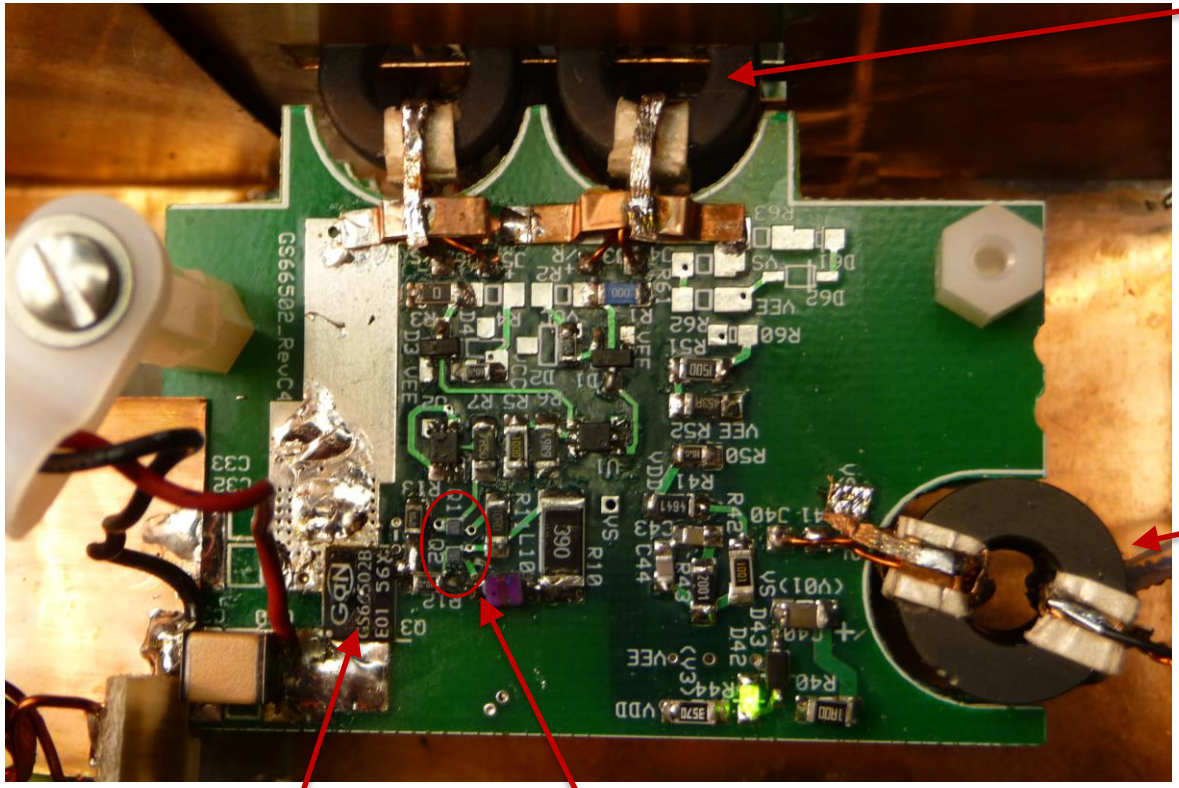
Trig. generator bd.



185 Ω load

Comp.
network

“Rev_C” driver board



Trigger transformers (2)

AC power transformer

GaN FET
GS66502
(GaN Systems)

eGaN FETs (2)
EPC2037 (EPC Corp.)

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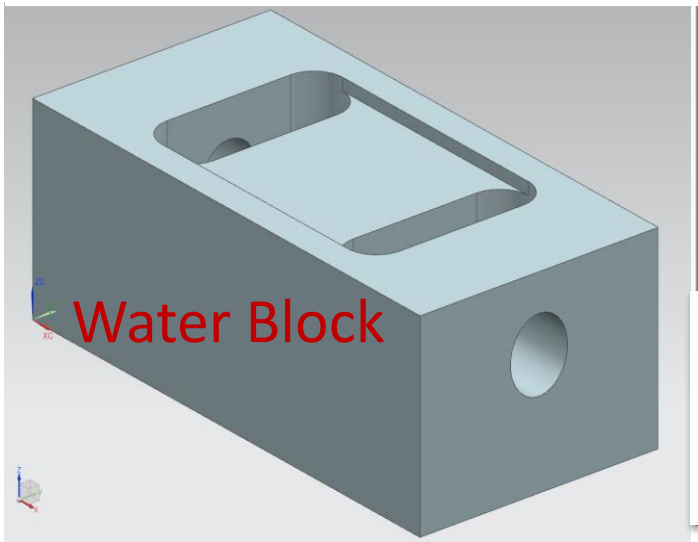
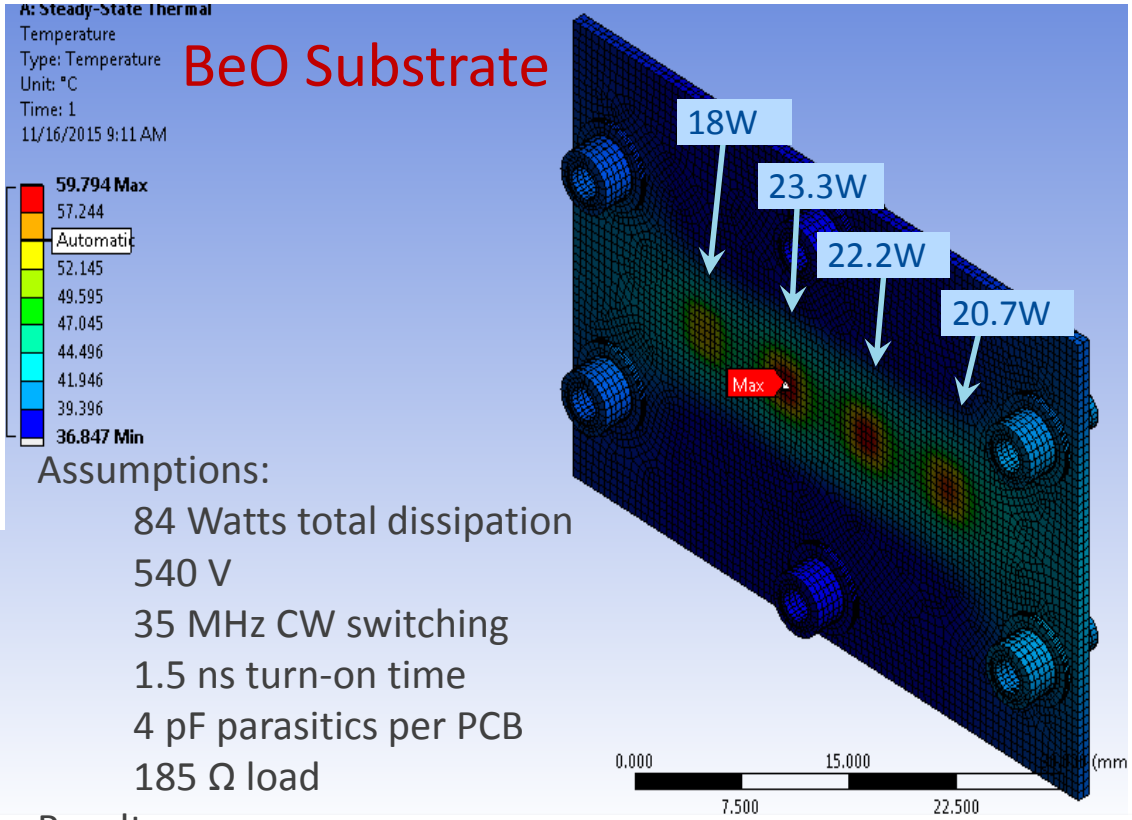
Estimating losses at high switching rates

- Made measurements to relate FET dissipation and T_j for various switching rates
  - Measure T_j directly with thermal imager
  - The FET case top surface temperature is T_j
- Verified my Mathcad spread sheet closely predicts FET losses for given switching conditions
  - Voltage and load
  - Number of FETs
  - Transition rates
  - Switching rate
  - Parasitic values
- Obtained Mathcad estimate for 35 MHz CW switching
- Consulted with Alex Chen to imagine a way to water cool a four-FET switch

Water cooling GaN FETs – ANSIS model (A. Chen, J. Leibowitz)

- 4 FETs soldered to metalized BeO substrate
  - .040” thick
  - 270 W/mK
- Water block mounted to BeO back side
- 28˚C water
- 0.1 gpm flow





Assumptions:

- 84 Watts total dissipation
- 540 V
- 35 MHz CW switching
- 1.5 ns turn-on time
- 4 pF parasitics per PCB
- 185 Ω load

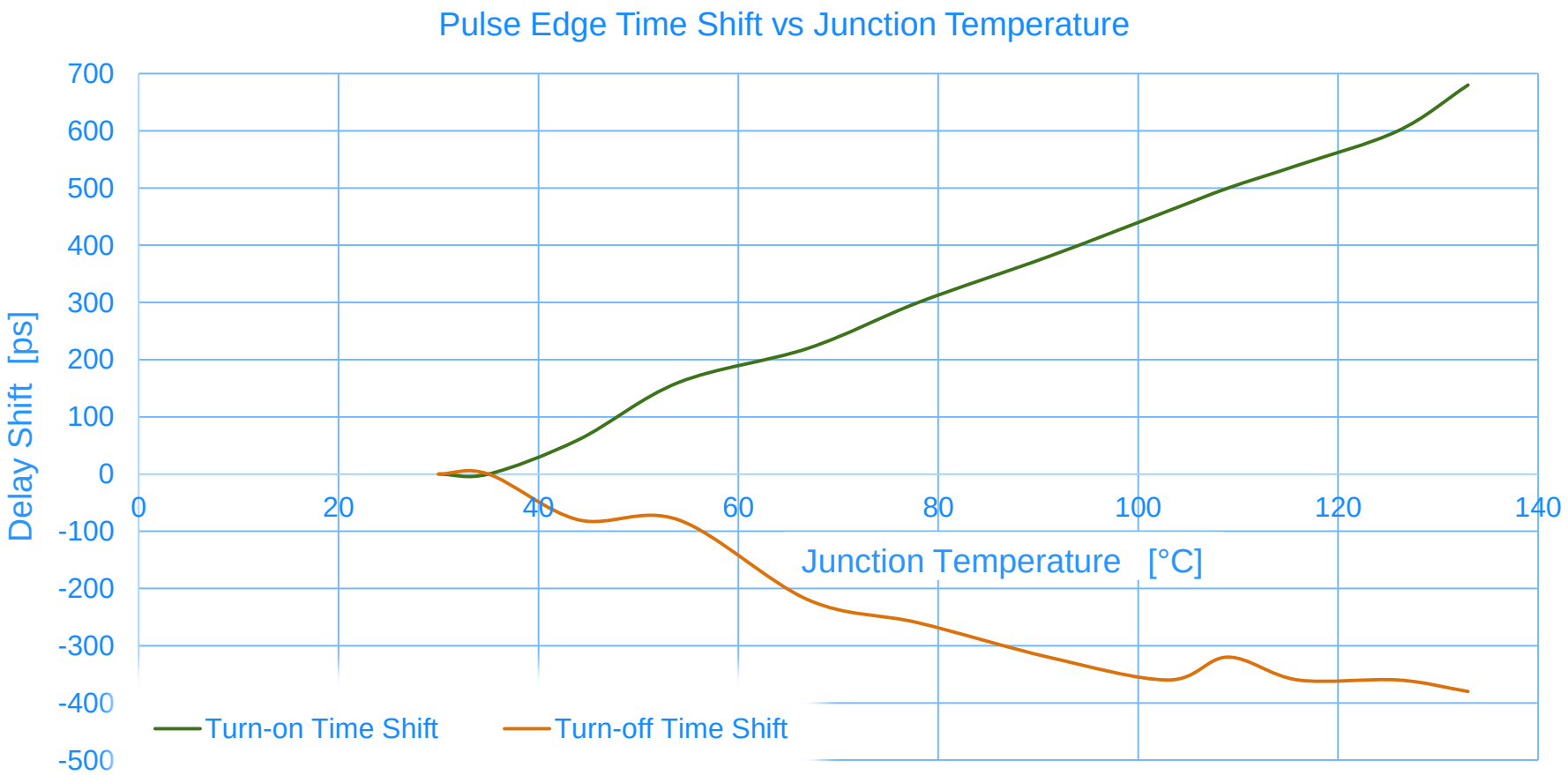
Results:

- Substrate temp: 60 – 57 ˚C
- T_j worst case = 108˚C (2˚C $R_{thj\text{-}c}$)

Timing effects with elevated FET junction temperature, T_j

- High repetition rate switching reveals only turn-on and turn-off edge timing shifts as T_j increases
  - There are no other adverse effects
  - Observed effect harmonizes with known gate threshold voltage positive temperature coefficient
- There is a time constant related to the time shifts
  - Bursts were made of varying number of pulses at 9 MHz switching rate
    - 9 MHz resulted in 133 T_j at steady state
  - Measurements of the time shifts were made of the pulse at the end of the burst intervals
  - Measurements can be made to determine thermal time constant
- Conceivable solution: A compensation algorithm (filter) can be implemented in the waveform generator
  - A function of both operating voltage and existing switching rate

Timing shifts with Junction Temperature



- Time shift value is measured at 95% max. amplitude

Conclusions

- The current multi-GaN FET scheme accomplishes (so far)
  - 500 V to 600 V operation
  - Well under 2 ns turn-on time
  - 2.2 ns flat top for kicking individual bunches
  - 81 MHz bursts
    - Compensation network is required with either high- or low-side switch topology
- Improvements are currently being made to trigger timing
- We yet have options regarding switch topology
- 35 MHz average rep rates seem possible with water cooling
  - Certainly worth prototyping
- High average switching temperature effects on the GaN FET should be able to be compensated out

END